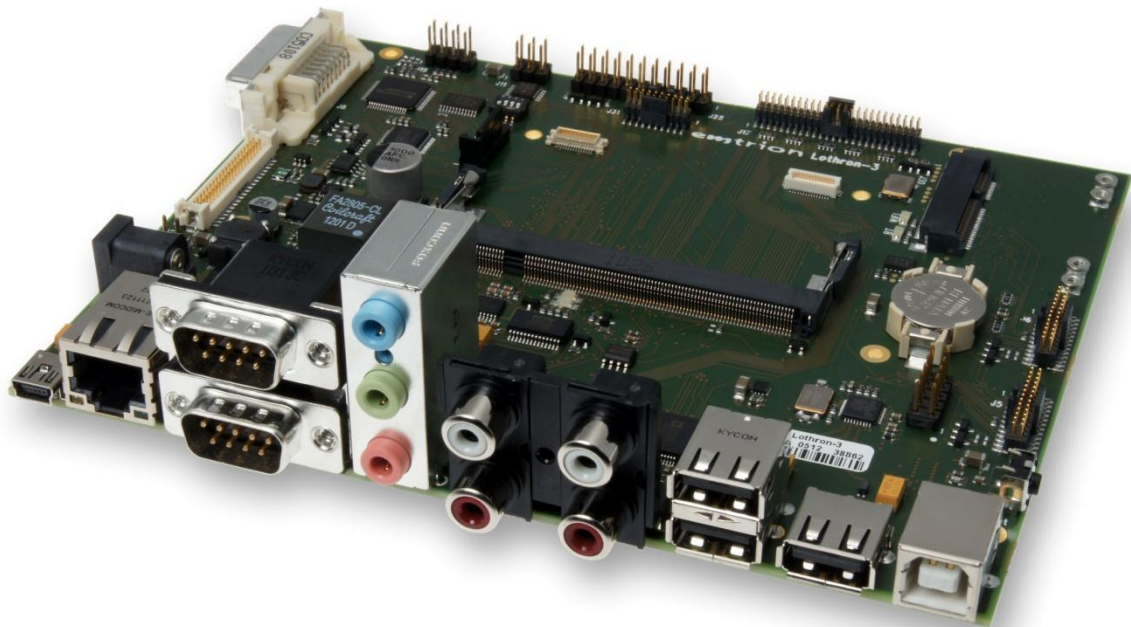


DIMM-Base Lothron

HiCO.DIMM compliant baseboard

Hardware Description

Rev7 / 04.03.2013



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Revision: **7 / 04.03.2013**

Rev	Date/Signature	Changes
1	31.01.2011/Sr	First revision
2	11.04.2011/Sr	- Product name "Lothron" changed to "DIMM-Base Lothron"
3	13.10.2011/Sr	Support for DIMM-MX53x CPU module added
4	01.03.2012/Sr	Document updated for the new hardware revision R3A: - Chapter "Block Diagram" updated - Chapter "Features and Specificities" updated - Chapter "First configuration" updated - Chapter "DIMM interface" updated - Chapter "Ethernet" updated - Chapter "WiFi" updated - Chapter "emCon-Ando – Extension Slot" added - Chapter "USB Host" updated - Chapter "SATA Interface" added - Chapter "DVI-Port": I2C address changed to 0x3F - Chapter "LVDS Interface" added - Chapter "Touch Screen Interface" added - Chapter "Display Identification and EDID" added - Chapter "CMOS Camera Interfaces" updated - Chapter "I2C I/O-Expander" updated - Chapter "I ² C-Bus" updated - Chapter "Keypad" added - Chapter "Power Sequencing" added - Chapter "Pin Assignment": SODIMM connector J1 changed; SODIMM Extension 2 J28 added; emCon-Ando Extension J30 added; SATA connector J27 added; LVDS connector J29 added; camera connectors J5 and J6 updated; Keypad connector J31 added; DC Power Jack added - Chapter "Dimensional Drawing" updated
5	06.07.2012	- Chapter "Pin Assignment": J17, CPU Bus Connector Pin 49 and 50 corrected.
6	13.11.2012	Support for DIMM-MX6x CPU module added DVI Display identification via I ² c removed in chapter 6.10.7 Added pin assignment of connectors DVI (J8), UART (J20), Ethernet J16 and USB (J3, J4, J7)
7	04.03.2013	- Chapter "CMOS Camera Interfaces, J5, J6": Wrong supply voltage in the description corrected

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1 Introduction

DIMM-Base Lothron is an extension board based on the DIMM [1] interface standard from emtrion. The board currently supports several core modules: DIMM-SH7723, DIMM-SH7724, DIMM-MX257, DIMM-MX53x and DIMM-MX6.

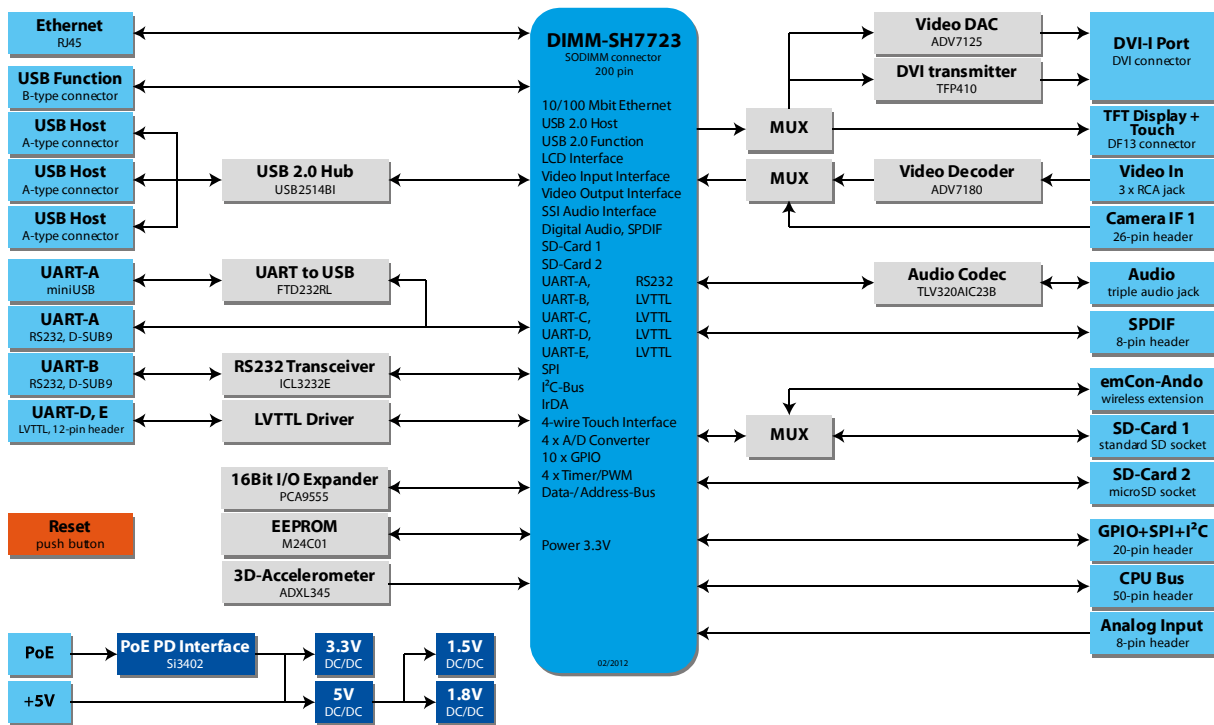
DIMM-Base Lothron is intended to be used as a development platform and demonstrates the capabilities of our core modules, as well as the advantages of the DIMM interface. Indeed, Lothron provides all connectors that are needed to make a full use of the core's features and also implements some additional features that will be controlled from the core module, thanks to the DIMM interface.

This Hardware manual describes the physical and electrical characteristics of the board. It covers the use of DIMM-Base Lothron with all supported Core modules but only gives additional details that are specific to the base. For this reason, it has to be used together with the manuals of the Core.

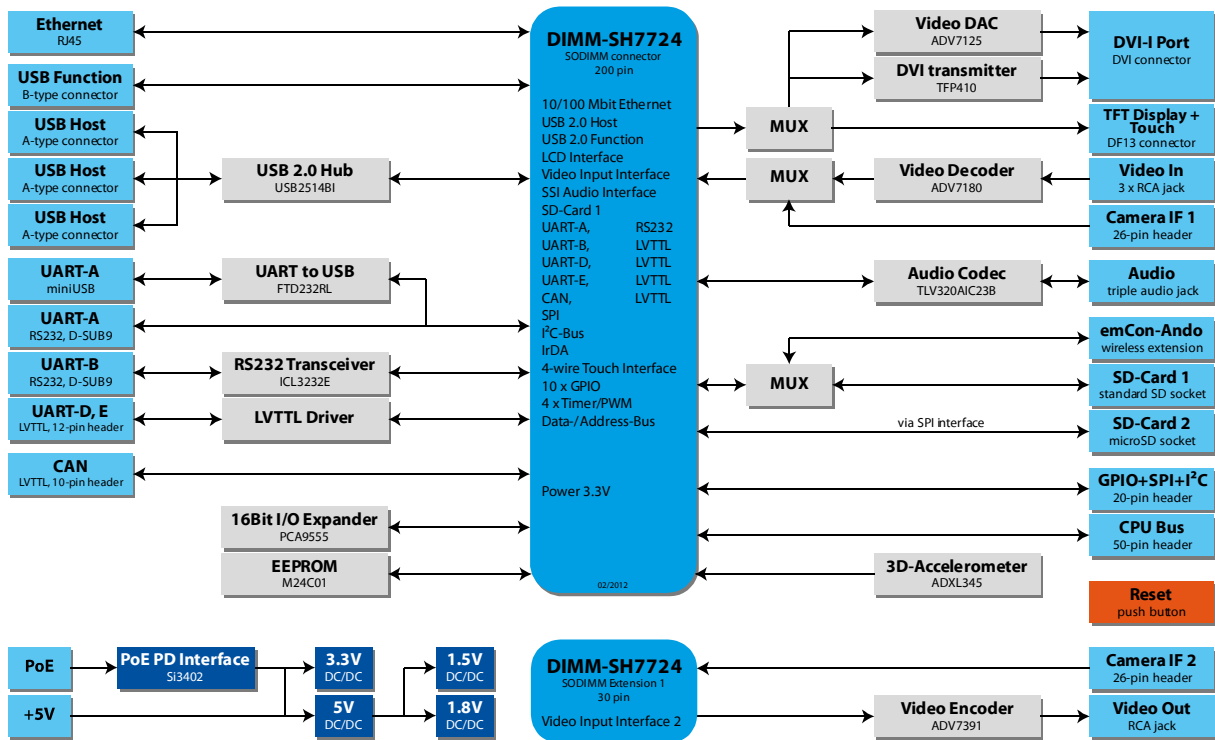
Most interfaces of the Lothron base board are common to all Core modules. Relevant differences between these boards are explicitly mentioned in this manual.

2 Block Diagram

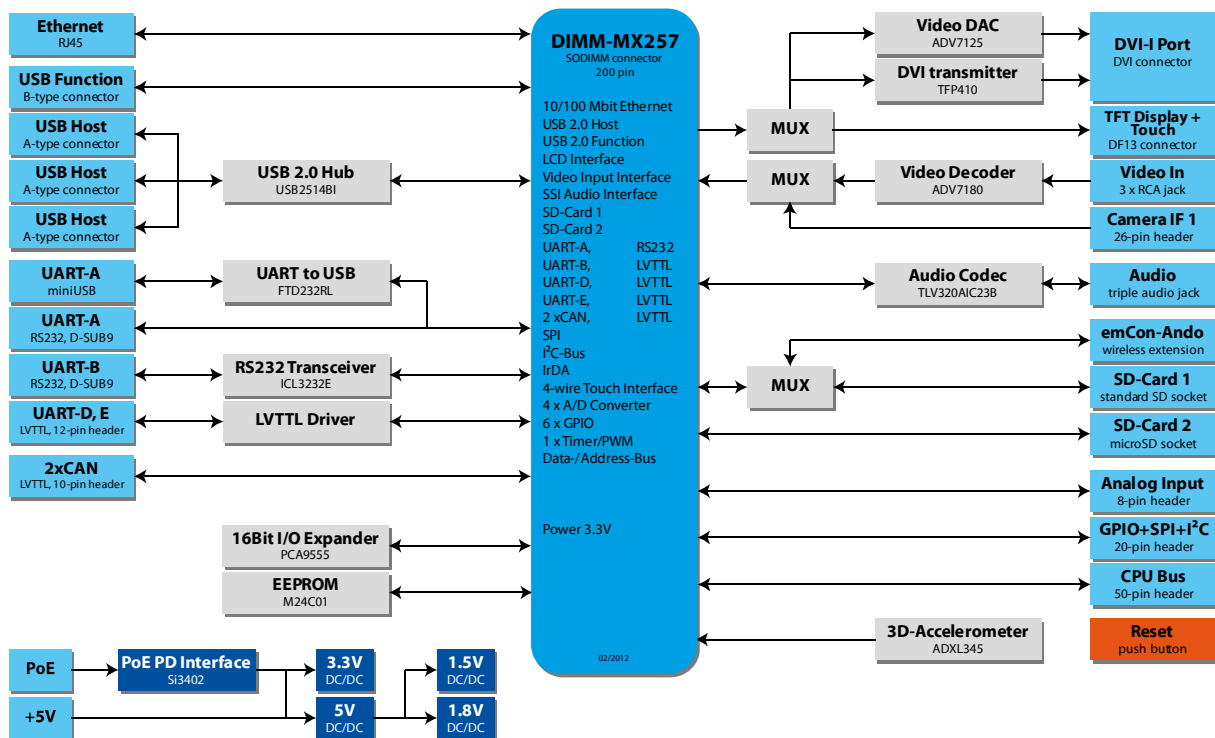
2.1 DIMM-SH7723



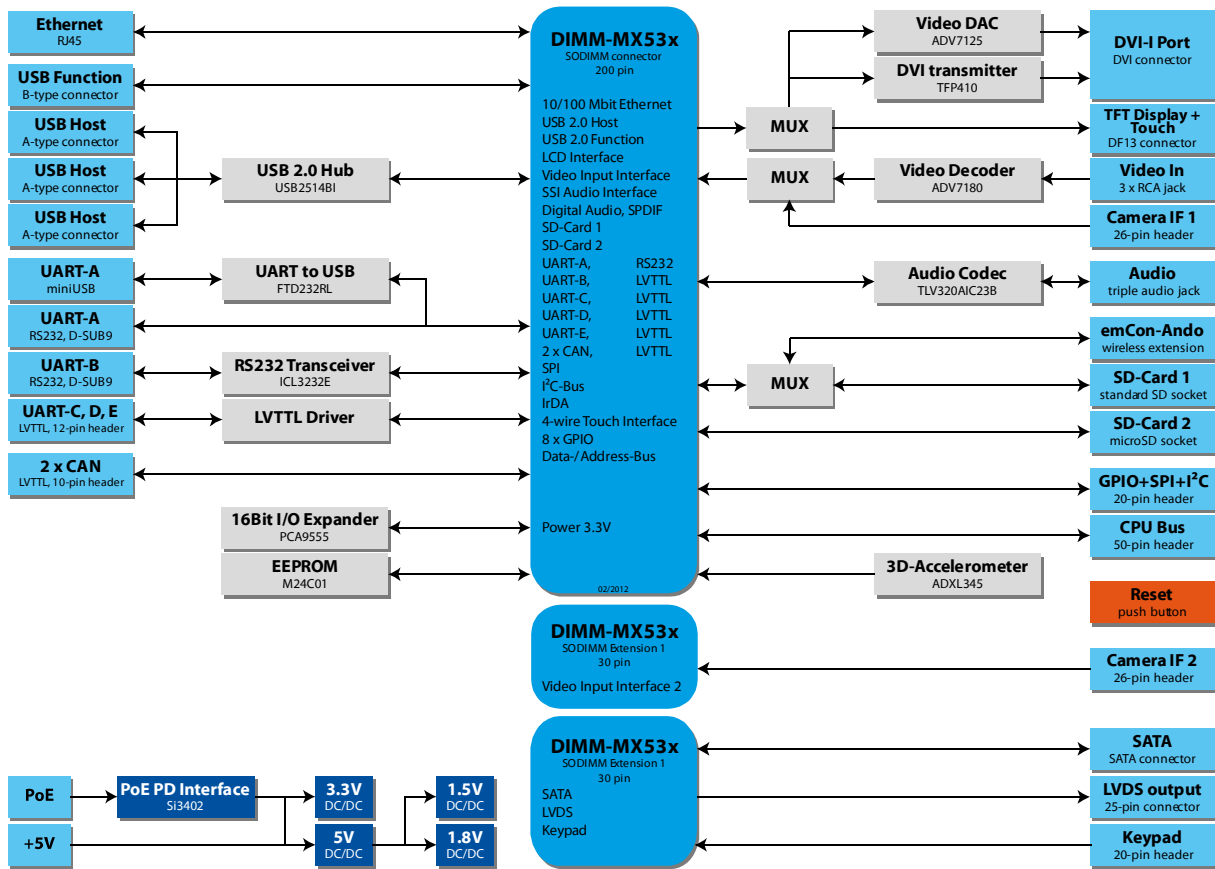
2.2 DIMM-SH7724



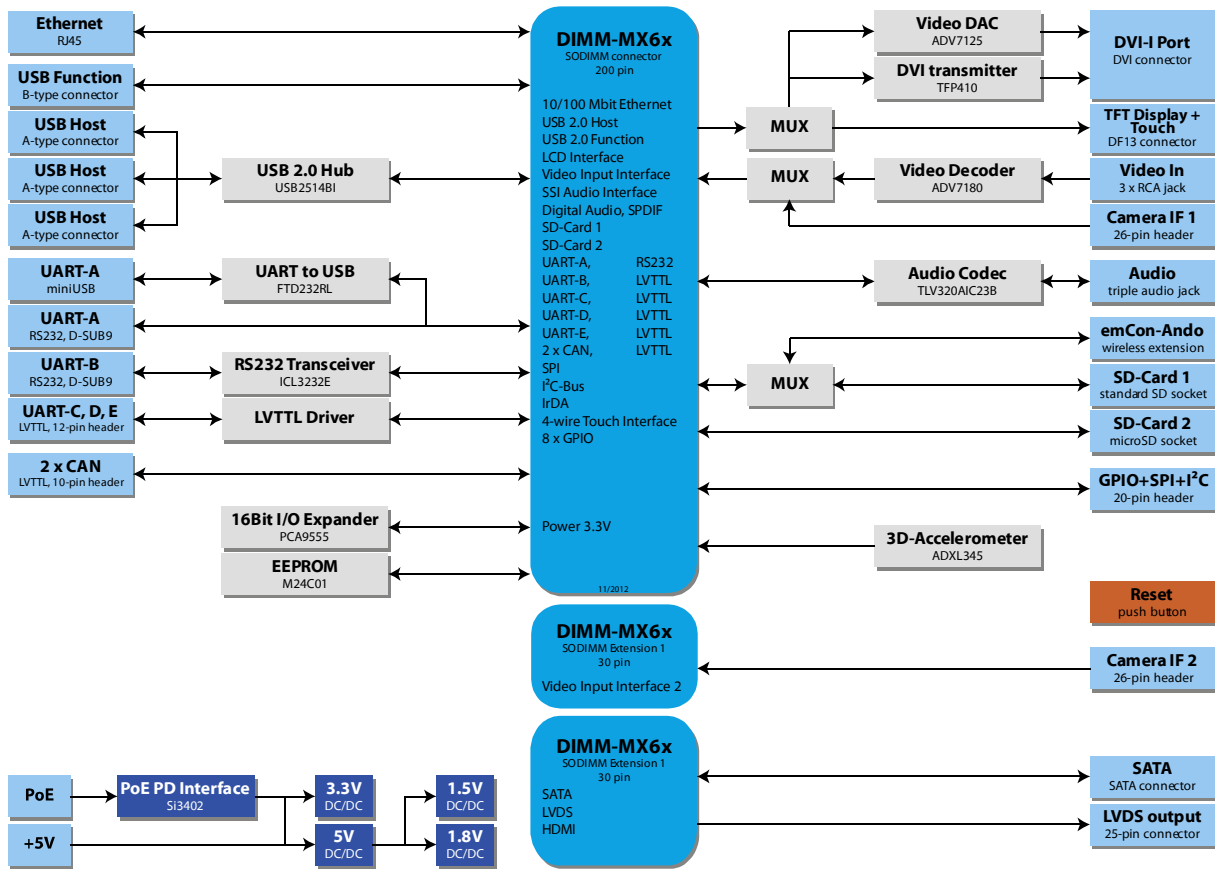
2.3 DIMM-MX257



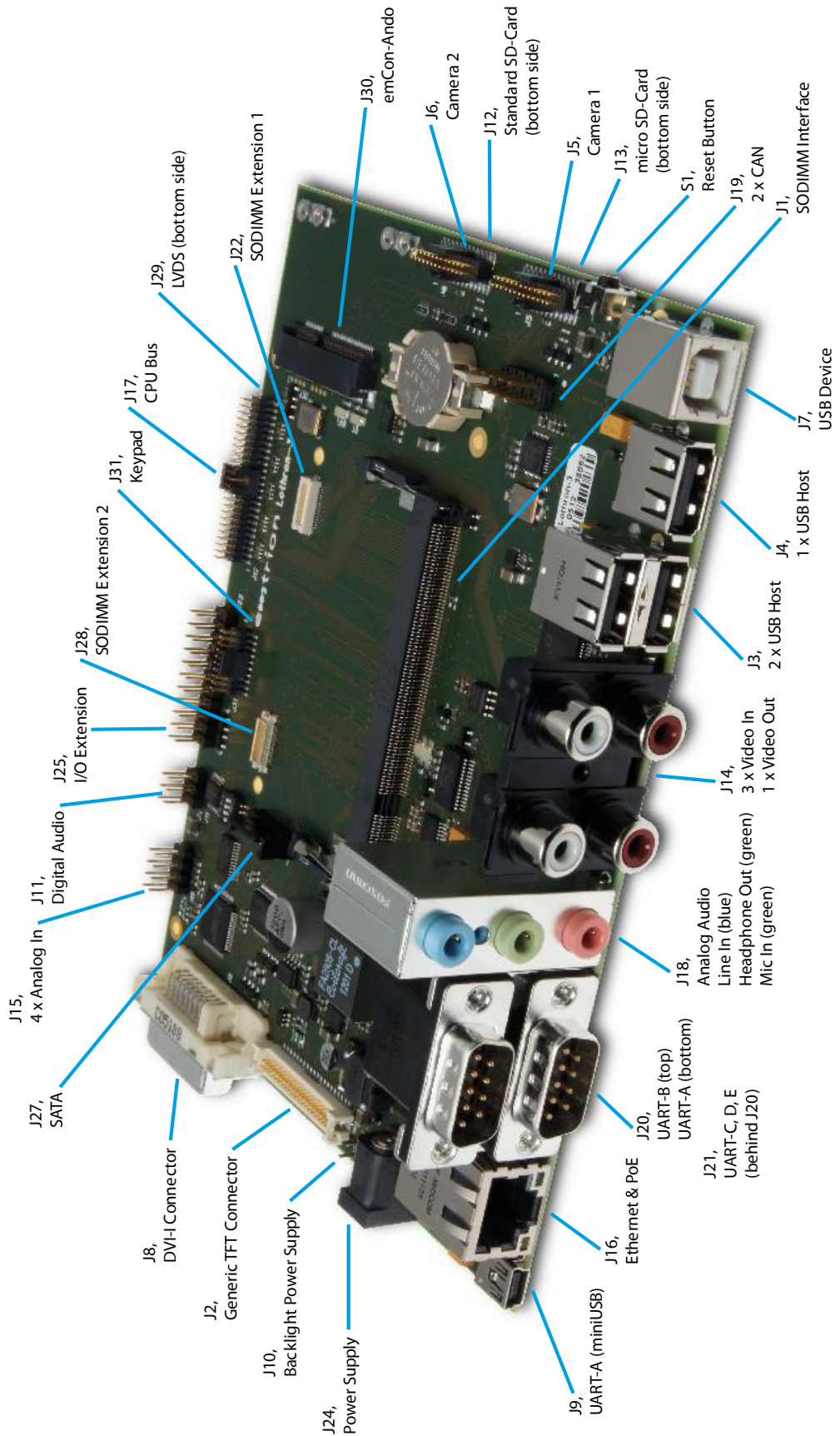
2.4 DIMM-MX53x



2.5 DIMM-MX6x



3 Connector Overview



4 Handling Precautions

Please read the following notes prior to installing CPU module to the DIMM-Base Lothron. They apply to all ESD (electrostatic discharge) sensitive components:

- Before installing a CPU module the Lothron base board needs to be configured depending on the used CPU module. Further information can be found later in this document.
- Before touching the base board it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) a CPU module, unplug the power cable from your mains supply.
- Also switch off the power supply before plug or unplug cables at not ESD protected connectors.
- Handle the board with care and try to avoid touching its components or tracks.

5 First Configuration

Before installing a CPU module do the following configuration:

5.1 Ethernet

Because of different Ethernet Controllers the voltage for the LAN transformer must be configured depending on the used CPU module. In the past this was done by a jumper. Since the hardware revision R3 the voltage can be configured by software automatically.

If your software doesn't support this feature yet you can set the voltage manually with the DIP-Switch 4 on the DIMM-Base Lothron. When the voltage is configured by software the DIP-Switch is overwritten and its position doesn't care.

The following table shows the position of the DIP-Switch according to the CPU module:

CPU module	Voltage	DIP4
DIMM-SH7723	1V8	OFF
DIMM-SH7724	3V3	ON
DIMM-MX257	3V3	ON
DIMM-MX53x	3V3	ON
DIMM-MX6x	3V3	ON

6 Functional Description

6.1 List of features

The DIMM-Base Lothron provides the following interfaces and functions. Depending to the used CPU module there will be some differences which are described later in the document.

- 200 pole SODIMM connector for processor modules
- 30 pole connector for SODIMM extension 1
- 30 pole high speed connector for SODIMM extension 2
- 10/100Base-Tx Ethernet interface at RJ45 jack
- Power over Ethernet PoE function, isolated
- emCon-Ando extension slot for wireless communication modules
- 1 x USB 2.0 Device interface at Type-B jack
- 3 x USB 2.0 Host interface at Type-A jack with USB 2.0 High Speed Hub
- DVI-I (digital & analog) connector for standard TFT or CRT monitors
- generic display interface for TFT displays with 18bpp including an interface for 4-wire resistive touch screens
- LVDS display interface
- switched 5 Volt power source for display backlight
- Video in decoder at three phono jacks (3 x Composite, 1 x S-Video or 1 x Component)
- Video out encoder at phono jack (1 x Composite)
- 2 generic camera interface for CMOS cameras
- analog audio with stereo headphone output, stereo line input and mic input at 3.5mm audio jacks
- digital audio input and output at 6 pin header
- 1 standard SD-Card socket
- 1 micro SD-Card socket
- 3D acceleration sensor
- up to 5 serial ports, two as RS232 at D-SUB-9 jack, the other as LVTTL
- RS232 to USB converter at a miniUSB jack
- Connector for two CAN channels (LVTTL), depending on the CPU module
- 22 pin header for SPI, I2C and GPIOs
- 50 pin header for data and address bus of the CPU module
- 16-Bit I2C-I/O-Expander for onboard functions
- I2C revision EEPROM
- pin header for analog inputs
- pin header for keypad interface
- 4-pole dip switch
- 1 reset button
- Battery holder for RTC backup, CR1632
- Power jack +5V

6.2 Features and Specificities

Most of the features which are available with DIMM-Base Lothron work as described on the cores hardware documentation because the base only provides connectors. However, the Lothron base board offers some additional features which are specific to it and which are documented in this manual. The table at the end of this section summarizes, for each core module and every feature that are available, which function is relying on the core modules and which is specific to DIMM-Base Lothron.

Legend:

“Core”: feature from the Core module; please refer to the Cores hardware documentation to know how to use it.

“Base”: feature is specific to the Lothron base board; all information on how to use it are given in the present manual

“NA”: not applicable; this feature is not available with the specified Core module

Feature	DIMM-SH7723	DIMM-SH7724	DIMM-MX257	DIMM-MX53x	DIMM-MX6x
Ethernet	Core	Core	Core	Core	Core
Power over Ethernet (PoE)	Base	Base	Base	Base	Base
emCon-Ando	Base ¹	Base ¹	Base ¹	Base ¹	Base ¹
USB 2.0 Host	3 ports Core/Base ²	3 ports Core/Base ²	3 ports Core/Base ²	3 ports Core/Base ²	3 ports Core/Base ²
USB 2.0 Device	Core	Core	Core	Core	Core
TFT Display (generic)	Core	Core	Core	Core	Core
LVDS Interface	n/a	n/a	n/a	Core	Core
Touch Screen	Core	Core	Core	Core	Core
DVI-I Port	Core/Base ³	Core/Base ³	Core/Base ³	Core/Base ³	Core/Base ³
Camera Input 1	Core	Core	optional ⁷	Core	Core
Camera Input 2	n/a	Core	n/a	Core	Core
Video Input	Core/Base ⁴	Core/Base ⁴	optional ⁷	Core/Base ⁴	Core/Base ⁴
Video Output	n/a	Core/Base ⁴	n/a	n/a	n/a
Analog Audio	Base	Base	Base	Base	Base
Digital Audio	Core	Core	n/a	Core	Core
SD-Card Socket	Core	Core	Core	Core	Core
microSD-Card Socket	Core	Core ⁵	Core	Core	Core
UART (-A, -B) RS232	Core ⁶	Core ⁶	Core ⁶	Core ⁶	Core ⁶

UART (-C, -D, -E) LVTTTL	3 ports Core	2 ports Core	2 ports Core	3 ports Core	3 ports Core
UART-A via miniUSB	Base	Base	Base	Base	Base
CAN	n/a	1 port Core	2 ports Core	2 ports Core	2 ports Core
SATA	n/a	n/a	n/a	1 port	1 port
SPI	1 port Core	1 port Core	1 port Core	1 port Core	1 port Core
I²C	1 port Core	1 port Core	1 port Core	1 port Core	1 port Core
IrDA Interface	Core	Core	n/a	3 ports Core ⁸	3 ports Core ⁸
GPIO	min. 4 GPIOs Core	10 GPIOs Core	6 GPIOs Core	8 GPIOs Core	8 GPIOs Core
Analog Inputs	4 inputs Core	n/a	4 inputs Core	n/a	n/a
Keypad	n/a	n/a	n/a	Core	n/a
3D Acceleration Sensor	Base	Base	Base	Base	Base
CPU-Bus Interface	16 x address; 16 x Data Core	16 x address; 16 x Data Core	16 x address; 16 x Data Core	11 x address; 16 x Data Core	n/a
Power On Sequencing	No ⁹	No ⁹	No ⁹	Yes	Yes

1: The emCon-Ando connector and the standard SD-Card socket are both connected to the first SDIO interface of the SODIMM connector. They cannot be used in parallel.

2: USB 2.0 Host Controller at the core module; 4-port USB Hub at baseboard

3: The graphic controller is located at the core module. The signal adaption for the DVI-I interface is done on the base board. The DVI-I interfaces and the generic TFT connector cannot be used at the same time.

- 4:** The core modules provide the video interfaces which control the video decoder/encoder placed at the base board.
- 5:** The interface is used in SPI mode.
- 6:** The RS232 transceiver for UART-A is placed on the core module; for UART-B the transceiver is placed at the base board.
- 7:** Please ask emtrion for more information.
- 8:** Every UART port can also be used as IrDA interface. At the DIMM-Base Lothron the three LVTTTL UART-Ports (C, D and E) can be used for IrDA. An IrDA transceiver must be added external.
- 9:** Works without power sequencing. No need for this CPU module.

6.3 DIMM interface, J1

The DIMM interface is a standardized interface between the DIMM CPU boards from emtrion and carrier boards. The interface consists of a 200 pin SODIMM connector with 2.5V keying which is commonly used for DDR1 memory modules [1].

All peripheral functions of the CPU boards and a memory bus interface are available at this connection. Also power is supplied via the SODIMM interface. Mechanical characteristics and a general pinout specification can be found later in this document. Individual differences of the CPU boards can be found in their appropriate manuals.

Watch:

The pin assignment is specific for the emtrion boards and must not be used for other boards.

6.3.1 SODIMM Extension 1

The DIMM-Base Lothron has an additional 30-pin connector J22 to extend the DIMM interface. This board-to-board connector is used for a second camera interface and a video output interface.

6.3.2 SODIMM Extension 2

Since the hardware revision R3 of the DIMM-Base Lothron a second extension connector J28 for high speed signals is added. This connector is used for SATA, LVDS and keypad interfaces.

6.4 Ethernet, J16

A 10/100 Mbit TX Ethernet interface is available via the RJ45 jack J16. The jack has integrated magnetics whose DC level can be sourced by 1.8V or 3.3V.

Because of different Ethernet Controllers the voltage for the LAN transformer must be configured depending on the used CPU module. In the past this was done by a jumper. Since the hardware revision R3 the voltage can be configured by software automatically.

If your software doesn't support this feature yet you can set the voltage manually with the DIP-Switch 4 on the DIMM-Base Lothron. When the voltage is configured by software the DIP-Switch is overwritten and its position doesn't care.

The following table shows the position of the DIP-Switch according to the CPU module:

CPU module	Voltage	DIP4
DIMM-SH7723	1V8	OFF
DIMM-SH7724	3V3	ON
DIMM-MX257	3V3	ON
DIMM-MX53x	3V3	ON
DIMM-MX6x	3V3	ON

To set the voltage by software the signal LAN_3V3#/1V8, which is connected to the 16 Bit [I2C-I/O-Expander](#) (Port1, I/O7), must be configured. A HIGH set the voltage to 1.8V, a LOW to 3.3V.

Two LEDs show the signal traffic (green) and 100 Mbit transfer speed (yellow).

6.5 Power over Ethernet (PoE)

The DIMM-Base Lothron can be used as Power over Ethernet (PoE) powered device (PD) and supplied via the Ethernet cable compliant to the IEEE 802.3 standard. As PoE PD interface the Si3402 from Silicon Labs is used, which includes all power management and control functions. The Si3402 is also used as an isolated flyback regulator and generates the 5V main voltage at the base board.

The maximum available power for the base board is 10 Watt. For further information see chapter [Power Supply](#).

To supply the DIMM-Base Lothron via PoE a Power Sourcing Equipment (PSE) is necessary, for example an Ethernet switch with PoE option.

6.6 WiFi

With the hardware revision R3 of the DIMM-Base Lothron the onboard WiFi module is replaced by a generic connector called **emCon-Ando**.

The electrical and mechanical details are specified by emtrion. For more information see the chapter "emCon-Ando - Extension Slot".

6.7 emCon-Ando – Extension Slot

The emCon-Ando Extension Slot is a generic connector to support several wireless communication standards on emtrion baseboards. The connector is a standard miniPCI-Express socket with an emtrion specific pin assignment. Parts of the pins are similar to the miniPCI-Express specification which is why some third-party half-size modules can be used as well as emtrion modules.

Please contact emtrion to get information about the supported modules.

emCon-Ando combines the following interfaces:

- USB-Host
- SDIO
- UART (only RX and TX signals)
- I²C Bus
- Reset, Power Down and Status Pins
- Power Supply (+3.3V, +1.8V, +1.5V)

6.7.1 USB-Host interface

As USB-Host interface one downstream port of the onboard USB Hub is used. Only the two differential data lines are connected.

6.7.2 SDIO interface

The SDIO interface is connected to the SD-Card interface (SDC1) of the SODIMM connector, together with the standard SD-Card socket J12. Because of this there are multiplexers used to switch between WiFi and SD-Card socket. The multiplexers are controlled by the signal *WIFI#/SDCARD*. A low will choose the WiFi module; a high the SDC socket.

There is also a small circuit to simulate unplugging and replugging of the SDC device. This can be helpful for the software during switching between WiFi and SD-Card. If the signal *SDC1_CD#_DISABLE* is switched to a high the card detect signal is disabled and simulates an unplugging of the SDC device. By switching *SDC1_CD#_DISABLE* back to low (default), the original card detect state is given to the CPU module.

Both signals, *WIFI#/SDCARD* and *SDC1_CD#_DISABLE*, can be controlled by an [I2C-I/O-Expander](#).

WiFi and the standard SD-Card socket J12 cannot be used simultaneously!

6.7.3 UART interface

As UART interface the UART_D from the UART connector J21 are used. The signals are connected to emCon-Ando and J21 without a multiplexer. The UART can either used by emCon-Ando or at J21, but not simultaneously.

6.7.4 I²C Bus

The global I²C Bus is connected via buffers to the emCon-Ando connector.

6.7.5 Reset

The global RESET# Signal is connected to the emCon-Ando connector.

6.7.6 Power Down

If the module supports power down states the pin *WLAN_BT_DISABLE#* can be used. A LOW sets the module in power down. At the DIMM-Base Lothron the pin is connected with the multiplexer control signal of the SDC interface *WIFI/SDCARD#*.

6.7.7 Status Pins

The two status pins for Bluetooth and WiFi activity connected to LEDs.

Activity	LED color
WiFi	Yellow
Bluetooth	Green

6.8 USB Host, J3, J4

The USB Host interface of the CPU board is connected to the upstream port of the USB 2.0 High Speed Hub USB2514BI from SMSC [3].

The downstream ports 1 - 3 are available at the USB Type-A connectors J3 and J4. The used EMC filters are dimensioned for High Speed Mode with 480 MBaud.

The downstream port 4 is connected to the emCon-Ando interface to support for example WiFi modules.

The VBUS output of the USB Host connectors are each controlled by an USB power switch. Every power switch can provide up to 5W. This will result in 15W for all four USB ports! The total power supply for the Lothron base board is limited to 10W! Depending to other connected peripherals, like displays, cameras etc., the user must decide how much power is available for USB devices.

The USB power switches can be controlled by the CPU module by the signal *USBH_PEN#*. Low switches the power on, a high (default) switch it off. An overcurrent is reported to the CPU by the signal *USBH_OC#*.

6.9 USB Device, J7

The USB device interface is available at the Type-B connector J7. The used EMC filters are dimensioned for High Speed Mode with 480 MBaud. All other characteristics depend on the CPU module.

6.10 Graphic Output

The DIMM-Base Lothron supports three interfaces to output graphic data. One is the DVI-I port which can drive standard computer monitors with DVI or CRT input. The second interface is a generic interface for TFT displays with RGB or 80-Series interface. Since the hardware revision R3 also a LVDS interface is available.

The DVI and RGB interfaces are limited to 18bpp color depth. Other parameters, like resolution or clocks, depend on the used CPU module.

The LCD signals are multiplexed between the DVI-I port and the generic display interface and can be switched with the signal *LCD_SELECT*. A low selects the DVI-I port; a high (default) the generic display interface. The signals *LCD_SELECT* can be controlled by an [I2C-I/O-Expander](#).

The LVDS interface is an independent display port to drive a second display for dual screen applications.

The DVI-I port and the generic display interface cannot be used simultaneously!

6.10.1 DVI-I Port, J8

Standard computer monitors can be connected to the DVI-I port which supports digital and analog graphic output.

The digital TMDS signals are generated by the TFP410 from TI [4] which only supports a single link connection. The pins for the second link are not connected at J8. The signal *DVI_RST#* can reset the TFP410 (low = reset) and can be controlled by the [I2C-I/O-Expander](#).

The I2C-Bus on DIMM-Base Lothron is connected to the TFP410 to configure or power down the chip. The 7-Bit chips address is 0x3F. The I2C-Bus also is connected to the DVI connector J8 via level converter to read specifications of the connected monitors.

The high speed video DAC ADV7125 from Analog Devices [5] converts the LCD signals from the CPU to analog signals to connect analog monitors. The chip doesn't need any configuration, but it can be powered down with the signal *CRT_PWRDWN#*. The signal is controlled by the [I2C-I/O-Expander](#). A low (default) sets the ADV7125 into power down mode.

6.10.2 Generic Display Interface, J2

The display interface J2 is a generic DF13-40 type connector that includes all signals needed to connect TFT displays with 18 bit color depth. It also includes signals for a 4-wire touch screen interface and an I2C interface.

For the touch screen interface please read the limitations in chapter “Touch Screen Interface”.

Please ask emtrion to find out which displays are supported.

6.10.3 LVDS Interface, J29

The LVDS interface is a 25-pin cable connector with a generic pin assignment. It includes four LVDS data pairs and one LVDS clock pair, I²C bus, touch screen signals and power supply.

The LVDS signals are directly routed to the CPU module. The chapter [Features and Specificities](#) shows which CPU modules support the LVDS interface.

For the touch screen interface please read the limitations in chapter “Touch Screen Interface”.

The +3,3V and + 5V power supply pins are only to supply the display controller or backlights from small displays. For display backlights with a large current consumption an external main supply must be used.

Voltage	Max. current
+3.3V	400mA
+5V	160mA

6.10.4 Touch Screen Interface

The DIMM-Base Lothron supports 4-wire resistive touch screen interfaces for the generic display interface J2 and the LVDS interface J29.

The emtrion CPU modules have only one touch controller to support one 4-wire resistive touch screen. This is why the touch screens of the two display interfaces are connected together. But you can connect only one touch screen at the same time! Either at the generic display interface or at the LVDS interface. If two touch screens are connected, this will corrupt the touch signals and result in invalid touch events.

If you need two independent touch screens please contact emtrion for a solution.

6.10.5 Backlight Supply, J10

The connector J10 is a 2 pin header which is intended to supply the power for the backlight of the connected generic TFT display. J10 is connected via a power switch to the +5V voltage. Before connecting a backlight, be sure not to exceed the maximum total power consumption of the DIMM-Base Lothron (10W). The power switch is controlled by the *LCD_DON* signal at pin 72 of the SODIMM connector. A low (default) at *LCD_DON* switch the voltage off, a high switch it on.

6.10.6 Spread Spectrum Oscillator

Normally the CPU clock is used as clock source for the LCD controller. But often displays have a big influence in EMC tests. Therefore a spread spectrum oscillator is provided on the DIMM-Base Lothron. A spread spectrum oscillator spreads the clock frequency in a specific domain, resulting in a signal with a wider bandwidth.

As default the DIMM-Base Lothron provides a 32MHz clock, which is spread by +/- 1,4%, at the SODIMM interface. The DIMM-SH7723 and DIMM-SH7724 CPU modules can use this clock as

external input for the LCD controller. At the DIMM-MX257 this function is not available. Please ask emtrion if other external clock frequencies are needed.

The switching between internal and external LCD clock can be done by software.

6.10.7 Display Identification and EDID

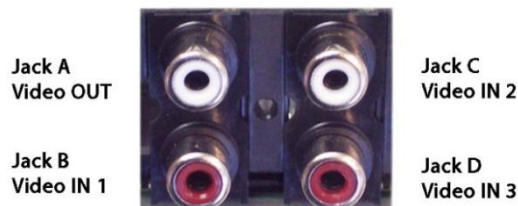
emtrion offers several displays with different formats, resolutions and properties. Every display needs its own timing for the data and control pins.

The switching is done automatically by the signal LCD_SELECT, which is used to switch the display data between the generic display connector and the DVI interface (see chapter [Graphic Output](#)). This means, that the EDID interface can't be read if the generic display interface is selected and vice versa.

6.11 Video Output, J14

The Lothron base board provides the video encoder ADV7391 [6] from Analog Devices. The encoder is connected to the 8-bit parallel VOU interface (4:2:2 YCbCr) of the SODIMM extension connector J22.

The video encoder supports Composite (CVBS) video out in NTSC and PAL mode at a RCA jack at the connector J14.



To configure the ADV7391 the I²C-Bus is used. The chip address is 0x2A. A 27 MHz clock is supplied to the VOU_CLKI pin of the SODIMM extension connector.

The RESET# input of the AD7391 is controlled by the *VOU_RST#* signal at pin 77 of the SODIMM connector.

6.12 Video Input and Camera Interface

The DIMM-Base Lothron provides a few options to capture images. The VIO1 interface of the SODIMM interface can be used either via a video decoder, which supports several input formats, or via a generic interface where a CMOS camera module can be connected.

It can be switch between video decoder and CMOS camera with multiplexers. To choose the video source the signal *VIO_SRC* of the SODIMM connector is used:

VIO_SRC	Source
0	CMOS camera J5
1	Video decoder

Additionally a second video input interface (VIO2) is provided via the SODIMM extension connector J22. At this interface is a second generic camera interface for CMOS cameras available.

Which interfaces are useable depends on the CPU module.

6.12.1 Video Input, J14

As video decoder the ADV7180 [7] from Analog Devices is used. The decoder is connected, via the described multiplexer, to the 8-bit parallel VIO1 interface (4:2:2 YCbCr) of the SODIMM connector.

Three 10 bit A/D converter of the ADV7180 are used to capture several input formats. Supported are 3 x composite (CVBS), 1 x s-video or 1 x component video signals in NTSC or PAL mode. The video source can be connected at RCA jacks at the connector J14.



The following ADCs of the ADV7180 are used:

Channel	ADC	RCA jack ¹
Composite 1		
CVBS	Ain1	B
Composite 2		
CVBS	Ain5	C
Composite 3		
CVBS	Ain4	D
S-Video (Y/C)		
Y	Ain1	B
C	Ain4	D
Component (YPrPb)		
Y	Ain1	B
Pr	Ain5	C
Pb	Ain4	D

¹ RCA jack A is used for video output.

To configure the ADV7180 the I²C-Bus is used. The 7-Bit chip address is 0x20.

The INTRQ# output of the decoder is routed to *IRQ_A* at pin 184 of the SODIMM connector. The RESET# input of the AD7180 is controlled by the *VIO_RST#* signal at pin 91 of the SODIMM connector. A low at *VIO_RST#* sets the chip into reset.

When the chip is not used it can be powered down by the signal *PWRDWN_ADV7180#*, which is controlled by the [I2C-I/O-Expander](#). A low at *PWRDWN_ADV7180#* sets the chip into power down mode. The default state is high.

6.12.2 CMOS Camera Interfaces, J5, J6

The DIMM-Base Lothron comes with two generic interfaces for CMOS cameras. As described before, the first interface J5 is multiplexed with the video decoder and connected to the VIO1 interface at the SODIMM connector. The second interface J6 is connected to the VIO2 interface at the SODIMM extension connector.

Both camera interfaces are generic interfaces at two 26 pole pin header J5 and J6 to connect CMOS camera modules. They include the 4:2:2 YCbCr interface with data and control signals, the I²C-Bus, power down and reset signals and the supply voltages 3.3 V and 5 V.

Since hardware revision R3 the main clock for the cameras is generated on the camera modules themselves.

As reset signal the global reset is used. If the used camera modules support the power down function, they can be powered down by the signals *PWRDWN_CAM1* (J5) and *PWRDWN_CAM2* (J6) controlled by the [I2C-I/O-Expander](#).

PWRDWN_CAMx	Mode
0	Running (default)
1	Powered down

Important note:

Because of problems with the signal integrity the pin assignment of the camera connectors has to be changed with the hardware revision R3! According to the used camera and baseboard maybe a cable adapter is necessary! Please contact emtrion or have a look to emtrions support pages for more information!

Please ask emtrion for details of supported CMOS camera modules.

6.13 Audio

6.13.1 Analog Audio

The DIMM-Base Lothron provides the high performance audio codec TLV320AIC23 [8]. The digital audio interface is connected to the SODIMM connector; the I²C-Bus (chip address 0x1B) is used for the control interface.

The codec provides a stereo headphone output (green, 30mW into a 32 Ω load), a stereo line input (blue) and a microphone input (red) at the triple 3.5mm audio jack J18.

As default the codec is configured as master and the CPU as slave. Since the hardware revision R3 the audio clock oscillator can be disabled to use the CPU as master (main clock is generated from the CPU). To disable the audio clock the signal *AUDIO_CLOCK_ENABLE*, which is provided by the [I2C-I/O-Expander](#) (Port1, IO6), has to be set to LOW.

6.13.2 Digital Audio

The SPDIF input and output signals from the SODIMM interface are routed via an impedance conversion and line drivers to the pin header J11.

6.14 SD-Card Socket, J12

A SD-Card socket J12 is available at the bottom side of DIMM-Base Lothron.

The socket is connected to the SD-Card interface (SDC1) of the SODIMM connector, together with the WiFi module. Because of this there are multiplexers used to switch between WiFi and SD-Card socket. The multiplexers are controlled by the signal *WIFI#/SDCARD*. A low will choose the WiFi module; a high the SDC socket.

There is also a small circuit to simulate unplugging and replugging of the SDC device. This can be helpful for the software during switching between WiFi and SD-Card. If the signal `SDC1_CD#_DISABLE` is switched to a high the card detect signal is disabled and simulates an unplugging of the SDC device. By switching `SDC1_CD#_DISABLE` back to low (default), the original card detect state is given to the CPU module.

Both signals, `WIFI#/SDCARD` and `SDC1_CD#_DISABLE`, can be controlled by an [I2C-I/O-Expander](#).

WiFi and the standard SD-Card socket J12 cannot be used simultaneously!

6.15 microSD-Card Socket, J13

A microSD-Card socket J13 is available at the bottom side of the board. All signals are directly connected to the SODIMM interface SDC2 without any further provisions. Thus the characteristics depend on the used CPU board.

6.16 CAN Interface, J19

Many of emtrion's CPU modules provide CAN controllers with up to two channels. At the Lothron base board the transmit and receive signals are routed together with 3,3V and GND to the pin header J19. The signals are in LVTTTL level without a CAN transceiver.

Ask emtrion for a cable adapter with including transceiver and D-SUB connector.

The following CPU modules supports CAN:

CPU module	CAN CH1	CAN CH2
DIMM-SH7723	n/a	n/a
DIMM-SH7724	Yes	n/a
DIMM-MX257	Yes	Yes
DIMM-MX53x	Yes	Yes
DIMM-MX6x	Yes	Yes

6.17 SATA Interface, J27

A standard SATA data connector is available next to the SODIMM connector. The differential data pairs are routed via the second SODIMM extension connector J28 directly to the CPU module.

A power connector for SATA is not available. The supply of current must be done by an external power supply unit.

The chapter [Features and Specificities](#) shows which CPU modules support the SATA interface.

The SATA connector is available since the hardware revision R3.

6.18 Serial Ports

The DIMM-Base Lothron supports up to 5 serial ports, depending on the used CPU module. The ports are named `UART_A` to `UART_E`.

`UART_A` and `UART_B` are available at the two D-SUB jacks J20 as standard RS232 interfaces. `UART_C`, `UART_D` and `UART_E` are connected with LVTTTL level to the pin header J21. The LVTTTL signals can be adapted to the customer's needs by adding the appropriate signal drivers (e.g.

RS232, RS548, RS422 etc.). By using the adapter cable ADA_RS232 from emtrion the LVTTTL signals also can be used as RS232 interface.

At UART_A additionally an UART-to-USB converter with a minUSB connector J9 is available. So the terminal interface UART_A can also be used with computers which have just USB and no COM ports. If a USB cable is connected to J9, UART_A is automatically switched to the USB interface. By unplugging the USB cable the RS232 interface at the D-Sub jack can be used.

Do not use the RS232 and USB cable at the same time. This will result in a corrupted communication.

The following UARTs are supported by the CPU modules:

DIMM-SH7723:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	SCIF3	RS232 transceiver on CPU module; can be used via USB
UART_B	RS232	-	SCIF5	RS232 transceiver on Lothron
UART_C	LVTTTL	-	SCIF4	
UART_D	LVTTTL	-	SCIF2	
UART_E	LVTTTL	-	SCIF1	

DIMM-SH7724:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	SCIF3	RS232 transceiver on CPU module; can be used via USB
UART_B	RS232	-	SCIF4	RS232 transceiver on Lothron
(UART_C)	LVTTTL	-	SCIF5	optional
UART_D	LVTTTL	-	SCIF2	
UART_E	LVTTTL	-	SCIF0	

DIMM-MX257:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	UART1	RS232 transceiver on CPU module; can be used via USB
UART_B	RS232	-	UART3	RS232 transceiver on Lothron
UART_D	LVTTTL	-	UART5	
UART_E	LVTTTL	-	UART2	

DIMM-MX53x:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	UART1	RS232 transceiver on CPU module; can be used via USB
UART_B	RS232	-	UART2	RS232 transceiver on Lothron
UART_C	LVTTTL	-	UART3	
UART_D	LVTTTL	-	UART4	
UART_E	LVTTTL	-	UART5	

DIMM-MX6x:

Port	Level	Handshake	CPU-IF	Remarks
UART_A	RS232	RTS, CTS	UART2	RS232 transceiver on CPU module; can be used via USB
UART_B	RS232	-	UART1	RS232 transceiver on Lothron
UART_C	LVTTTL	-	UART3	
UART_D	LVTTTL	-	UART4	
UART_E	LVTTTL	-	UART5	

6.19 I/O Extension, J25

The 22 pin header J25 includes up to 10 GPIOs, one SPI interface and an I²C-Bus interface. The I²C-Bus interface is decoupled to the onboard bus devices via a repeater circuit. At the I/O Extension the SCL and SDA lines are pulled up with 3.3-K resistors to 3.3V. All other signals are directly connected with the SODIMM connector. Their individual characteristics depend on the used CPU board. See the connector description later in this manual.

6.20 3-Axis Accelerometer

The ADXL345 [10] from Analog Devices is a 3-axis, digital accelerometer with high resolution (13-bit) measurement at up to +/- 16g. It measures the static acceleration of gravity, as well as dynamic acceleration resulting from motion or shock.

The chip is connected to the I²C bus with the 7-Bit address 0x1D. The IRQ output is connected to *IRQ_B* at the SODIMM connector, but can be disconnected by removing a series resistor if *IRQ_B* is used for other applications.

6.21 I²C Bus

At the DIMM-Base Lothron are several I²C-Bus clients:

Device	Slave	Chip Address (7Bit)
Audio Codec	TLV320AIC23	0x1B
Video Encoder	ADV7391	0x2A
Video Decoder	ADV7180	0x20
LCD to LVDS converter	TFP410	0x3F
16Bit I/O-Expander	PCA9555	0x26
EEPROM board revision	24LC01B	0x51
3D-Accelerometer	ADXL345	0x1D
Generic LCD Interface	PCA8574APW	0x3A
DVI EDID Interface	DVI-IF	0x3A or 0x50
Camera 1 Interface	CAM1-IF	Depends on used camera
Camera 2 Interface	CAM2-IF	Depends on used camera
CPU Bus Interface	CPU-Bus IF	Undefined

Further addresses are allocated by I²C devices used at the CPU modules. Please refer to the hardware manual of the used CPU module.

At all connectors with I²C-Bus interface the SCL and SDA line is decoupled to the onboard bus devices via a repeater circuit and the external SCL and SDA lines are pulled up with 3.3-K resistors to 3.3V.

At the DVI interface the I²C-Bus interface is decoupled to the onboard bus devices via a repeater circuit and the external SCL and SDA lines are pulled up with 4.7-K resistors to 5V.

6.22 I²C I/O-Expander

At the Lothron base board are several signals for example to switching multiplexers, change operating modes or just to read status information. These signals are controlled the 16-Bit I²C I/O expander PCA9555PW [9] from NXP. The chip is connected to the I²C Bus and configured to the 7-Bit address 0x26.

The interrupt output INT# is unused.

The following table shows the use of the I/O pins:

Port 0	Direction	Signal	Description
I/O 0	Output	PWRDWN_CAM1	Power down mode for CMOS camera 1
I/O 1	Output	PWRDWN_CAM2	Power down mode for CMOS camera 2
I/O 2	Output	PWRDWN_ADV7180#	Power down mode for video decoder
I/O 3	Output	CRT_PWRDWN#	Power down mode for analog outputs of DVI interface
I/O 4	Output	DVI_RST#	Power down mode for TFP410 LVDS converter of DVI interface
I/O 5	Input	DVI_MSEN	Hotplug detection for DVI interface
I/O 6	Output	LCD_SELECT	Selects generic LCD port or DVI port for graphic output
I/O 7	Input	AC_PRESENT	Shows the actual power supply (AC adapter or Power over Ethernet)

Port 1	Direction	Signal	Description
I/O 0	Input	MINIUSB_PRESENT	Shows whether miniUSB is plugged in
I/O 1	Output	EEPROM_WP	Write protection for revision EEPROM
I/O 2	Output	WiFi#/SDCARD	Selects WiFi module or SD-Card
I/O 3	Output	SDC1_CD#_DISABLE	Disables Card detection for SD-Card and WiFi module
I/O 4	Input	DIP1	DIP Switch 1 (0=OFF; 1 = ON)
I/O 5	Input	DIP2	DIP Switch 2 (0=OFF; 1 = ON)
I/O 6	Output	AUDIO_CLK_ENABLE	DIP Switch 3 (0=OFF; 1 = ON)
I/O 7	Output	LAN_3V3#/1V8	Sets the Ethernet voltage.

For detailed description of the signals see the description of the corresponding interface.

6.23 I²C Revision EEPROM

The CPU module can detect the type and revision of the base board by reading an EEPROM connected to the I²C bus. The 7-Bit address is 0x51. The write protection of the EEPROM is controlled by the signal *EEPROM_WP* of the [I²C-I/O-Expander](#). With a high level (default) the EEPROM is protected, with a low it is writeable.

6.24 CPU Bus Interface, J17

The data and address bus of the CPU module including control signals and I²C bus are routed to a 50 pin header. This interface can be used to add customer specific extension boards.

To minimize noises at the CPU bus there are series resistors added. The I²C-Bus interface is decoupled to the onboard bus devices via a repeater circuit and the SCL and SDA lines at J17 are pulled up with 3.3-K resistors to 3.3V.

It depends on the used CPU module which signals are available. The following table shows maximum possible signals:

Signal	Function
A[15:0]	16 address lines
D[15:0]	16 data lines
CKIO	Bus clock for synchronous transfers
RD#	Read strobe [low active]
WE0#	Write strobe lower byte [low active]
WE1#	Write strobe upper byte [low active]
CS#	Chip select [low active]
WAIT#	Wait signal for slow bus devices [low active]
IRQ_B	IRQ_B of SODIMM connector
BS#	Bus start, SH specific control signal [low active]
RESET#	Global reset output [low active]
I2C_SCL	I ² C bus clock signal
I2C_SDA	I ² C bus data signal

6.25 Analog Inputs, J15

Depending on the CPU module are up to four analog inputs at the 8 pin header J15 available. See the connector description later in this manual. Their individual characteristics depend on the used CPU board.

Each channel has a 100 Ohm series resistors implemented.

6.26 Keypad, J31

With the second SODIMM Extension connector J28 also 8 pins for a keypad are defined. The pins are routed directly to the pin header J31.

To see which CPU modules supports this interface please have a look at chapter [Features and Specificities](#).

6.27 DIP-Switch

The DIMM-Base Lothron provides a 4-pole DIP switch. The switches have no hardware specific function and can be read from the [I2C-I/O-Expander](#).

Since hardware revision R3 DIP3 is out of function and DIP4 is used the configuration of the Ethernet voltage.

6.28 Reset Switch, S1

A reset button S1 is placed at the right side of the DIMM-Base Lothron. A reset of the CPU module (e.g. by a software reset) also resets the Lothron base board.

6.29 Power Supply

The DIMM-Base Lothron can be supplied either by a +5Volt, +/- 5%, max. 2 A, wall adapter or by Power over Ethernet (PoE). The switching between the two power supplies is done automatically and without any dropouts during operating.

The actual power supply is indicated by the signal *AC_PRESENT* which is connected to the [I2C-I/O-Expander](#).

AC_PRESENT	Power Supply
0	Power over Ethernet
1	5V wall adapter

6.29.1 Onboard Regulators

The DIMM-Base Lothron has switching regulators for +5V (USB Host, Backlight, DVI interface), +3,3V (most of the base board functions and the CPU module), +1,8V (video codecs, WiFi, cameras, Ethernet) and +1,5V (emCon-Ando Extension Slot).

The 5V and 3,3V regulator each have a green LED to show the status of the voltages on the board. If the LEDs are on, the voltages are good.

6.29.2 Power Sequencing

Because of the power sequencing requirements of emtrions new CPU modules the power supply topology was changed with the hardware revision R3 of the DIMM-Base Lothron.

By plugging in the main adapter or PoE cable only the +3.3V regulator is enabled and supply one pin of the SODIMM interface called 3V3_CPU. This voltage is used on CPU modules to trigger the power sequencing. At this time all other voltages at the CPU module and the baseboard are disabled.

The CPU module can now switch on the main +3.3V voltage with the SODIMM signal POWER_ON_BASE (Pin 135). A HIGH at this signal will switch on a MOSFET which supply the main 3.3V for the CPU and base board. At the same time the +5V regulator is enabled which supplies all other voltage regulators. All voltages in the system are now enabled.

By using CPU modules that don't support the power sequencing feature, all voltages are enabled at the same time. The circuit is downwards compatible.

If the DIMM-Base Lothron is powered on without a CPU module is mounted, only the 3V3_CPU voltage is enabled and the power LEDs are off.

6.29.3 Power Consumption

The maximum available power for the complete system must not exceed 10W!

Important note:

Please make sure your connected devices like display, USB devices, cameras etc. including the DIMM-Base Lothron and the CPU module don't exceed the **10 Watt** limit! Otherwise this can damage your system!

6.29.4 Backup Battery

A battery holder J23 for lithium tab battery CR1632 is available to supply the RTC of the CPU boards.

7 Pin Assignments

7.1 J1, SODIMM connector

Type 200 pin SODIMM socket, 0.6 mm Pitch, 2,5V keying

Pin	Signal	Interface		Signal	Pin	
1	SPEED_LED#	Ethernet	USB Host	USBH_PEN#	2	
3	ETH_TDP			USBH_OC#	4	
5	ETH_TDM			USBH_DM	6	
7	GND			USBH_DP	8	
9	ETH_RDP			USB Device	USBF_VBUS	10
11	ETH_RDM				USBF_DM	12
13	LINK_LED#		USBF_DP		14	
15	USBH_VBUS		USB Host	Power	GND	16
17	CAN_TX		CAN	UART-A	UART-A_TXD#	18
19	CAN_RX	UART-A_RXD#			20	
21	UART-E_TXD	UART-E	UART-A_RTS#		22	
23	UART-E_RXD		UART-A_CTS#		24	
25	UART-D_TXD	UART-D	Touch		Touch_XP	26
27	UART-D_RXD				Touch_XM	28
29	UART-C_TXD	UART-C		Touch_YP	30	
31	UART-C_RXD			Touch_YM	32	
33	UART-B_TXD	UART-B	A/D	ANA1	34	
35	UART-B_RXD			ANA2	36	
37	ANA4	A/D		ANA3	38	
39	+3V3	Power		GND	40	
41	LCD_D22	LCD		LCD_D23	42	
43	LCD_D20			LCD_D21	44	
45	LCD_D18			LCD_D19	46	
47	LCD_D16			LCD_D17	48	
49	LCD_D14			LCD_D15	50	
51	LCD_D12			LCD_D13	52	
53	LCD_D10			LCD_D11	54	

55	LCD_D8		LCD_D9	56	
57	LCD_D6		LCD_D7	58	
59	LCD_D4		LCD_D5	60	
61	LCD_D2		LCD_D3	62	
63	LCD_D0		LCD_D1	64	
65	+3V3	Power		GND	66
67	LCDRD#	LCD		LCD_LCLK	68
69	LCD_DISP			LCD_DCK	70
71	LCD_HSYN			LCD_DON	72
73	LCD_VSYN			LCD_VCPWC	74
75	n/c			LCD_VEPWC	76
77	VOU_RST#	VIO0, VOU		VIO0_D7	78
79	VIO0_FLD			VIO0_D6	80
81	VIO_CKO			VIO0_D5	82
83	VIO0_CLK			VIO0_D4	84
85	VIO0_HD			VIO0_D3	86
87	VIO0_VD			VIO0_D2	88
89	VIO_SRC			VIO0_D1	90
91	VIO_RST#			VIO0_D0	92
93	+3V3	Power		GND	94
95	SDC2_D0	SDC2	SDC1	SDC1_D0	96
97	SDC2_D1			SDC1_D1	98
99	SDC2_D2			SDC1_D2	100
101	SDC2_D3			SDC1_D3	102
103	SDC2_CMD			SDC1_CMD	104
105	SDC2_CLK			SDC1_CLK	106
107	SDC2_CD#			SDC1_CD#	108
109	SDC2_WP# (GND)	SDC1_WP#	110		
111	SPI_SS#	SPI		SPI_MISO	112
113	SPI_SCK			SPI_MOSI	114
115	SCL	I2C	Audio	AUDIO_BCK	116
117	SDA			AUDIO_LRC	118

119	SPDI	SPDIF	AUDIO_DATI	120
121	SPDO		AUDIO_DATO	122
123	GND	Power	AUDIO_MCLK	124
125	GPIO8	GPIO	GPIO9	126
127	GPIO6		GPIO7	128
129	GPIO4		GPIO5	130
131	GPIO2		GPIO3	132
133	GPIO0		GPIO1	134
135	POWER_ON_BASE	Power	GND	136
137	n/c	Address A[15:0]	n/c	138
139	n/c		n/c	140
141	n/c		n/c	142
143	n/c		n/c	144
145	A14		A15	146
147	A12		A13	148
149	A10		A11	150
151	A8		A9	152
153	A6		A7	154
155	A4		A5	156
157	A2	A3	158	
159	A0	A1	160	
161	+3V3	Power	GND	162
163	D14	Data D[15:0]	D15	164
165	D12		D13	166
167	D10		D11	168
169	D8		D9	170
171	D6		D7	172
173	D4		D5	174
175	D2		D3	176
177	D0		D1	178
179	CKIO	Bus Control	n/c	180
181	BS#		n/c	182

183	RD#		IRQ_A	184
185	n/c		IRQ_B	186
187	WE0#		NMI	188
189	WE1#		RESO#	190
191	n/c		RESI#	192
193	n/c		n/c	194
195	WAIT#		n/c	196
197	CS#		n/c	198
199	BAT	Power	GND	200

7.2 J22, SODIMM Extension Connector 1

Type: 30-pin connector, Hirose DF12(3.0)-30DP-0.5V (header)

Pin	Signal	Pin	Signal
1	GND	2	+3.3 V
3	VOU_D7	4	VIO1_D7
5	VOU_D6	6	VIO1_D6
7	VOU_D5	8	VIO1_D5
9	VOU_D4	10	VIO1_D4
11	VOU_D3	12	VIO1_D3
13	VOU_D2	14	VIO1_D2
15	VOU_D1	16	VIO1_D1
17	VOU_D0	18	VIO1_D0
19	GND	20	GND
21	VOU_CLKI	22	VIO1_CLK
23	VOU_CLK	24	VIO1_FLD
25	VOU_VSYNC	26	VIO1_VD
27	VOU_HSYNC	28	VIO1_HD
29	GND	30	+3.3 V

7.3 J28, SODIMM Extension Connector 2

Type: 30-pin connector, Molex 53748-0308

Pin	Signal	Pin	Signal
1	SATA_RXN	2	LVDS_TX2_N
3	SATA_RXP	4	LVDS_TX2_P
5	SATA_TXP	6	LVDS_TX0_N
7	SATA_TXN	8	LVDS_TX0_P
9	GND	10	GND
11	KEYPAD_ROW1	12	LVDS_TX1_N
13	KEYPAD_COL1	14	LVDS_TX1_P
15	KEYPAD_ROW0	16	GND
17	KEYPAD_COL0	18	LVDS_CLK_N
19	KEYPAD_ROW2	20	LVDS_CLK_P
21	KEYPAD_ROW2	22	GND
23	KEYPAD_COL3	24	LVDS_TX3_N
25	KEYPAD_COL3	26	LVDS_TX3_P
27	Reserved	28	GND
29	Reserved	30	Reserved

7.4 J30, emCon-Ando - Extension Slot

Type: miniPCI-express connector : JAE MM60-52B1-G1

Pin	Signal	Pin	Signal
1	n/c	2	+3.3V
3	n/c	4	GND
5	n/c	6	+1.5V
7	n/c	8	+1.8V
9	GND	10	n/c
11	WIFI_SD0	12	n/c
13	WIFI_SD1	14	n/c
15	GND	16	+1.8V
17			
17	n/c	18	GND
19	n/c	20	WLAN_BT_DISABLE#
21	GND	22	RESET#
23	WIFI_SD2	24	+3.3V
25	WIFI_SD3	26	GND
27	GND	28	+1.5V
29	GND	30	SCL
31	WIFI_CLK	32	SDA
33	WIFI_CMD	34	GND
35	GND	36	USB DM4
37	GND	38	USB DP4
39	+3.3V	40	GND
41	+3.3V	42	n/c
43	GND	44	LED_WIFI_ACTIVE#
45	UART RTS ¹	46	LED_BT_ACTIVE#
47	UART_D_RXD	48	+1.5V
49	UART_D_TXD	50	GND
51	UART CTS ¹	52	+3.3V

1.) UART RTS and CTS are connected together on the baseboard.

7.5 J2, Generic TFT Connector

Type: 40 pin connector, Hirose DF13-40, 1.25 mm * 1.25 mm pitch

Pin	Signal	Pin	Signal
1	LCD VEPWC	2	LCD VCPWC
3	SDA	4	SCL
5	n/c	6	n/c
7	TFT_VCC	8	TFT_VCC
9	DE	10	GND
11	BLUE5	12	BLUE4
13	BLUE3	14	BLUE2
15	BLUE1	16	BLUE0
17	GND	18	GREEN5
19	GREEN4	20	GREEN3
21	GREEN2	22	GREEN1
23	GREEN0	24	GND
25	RED5	26	RED4
27	RED3	28	RED2
29	RED1	30	RED0
31	GND	32	VSYNC
33	HSYNC	34	DOTCLK
35	GND	36	TFT_VCC
37	Touch XP	38	Touch YP
39	Touch XM	40	Touch YM

7.6 J29, LVDS connector

Type: JAE FI-S25P-HFE

Pin	Signal	Pin	Signal
1	+3.3V (fused)	14	GND
2	+3.3V (fused)	15	LVDS_CLK_N
3	SCL	16	LVDS_CLK_P
4	SDA	17	GND
5	GND	18	LVDS_TX3_N
6	LVDS_TX2_N	19	LVDS_TX3_P
7	LVDS_TX2_P	20	GND
8	GND	21	TOUCH_XP
9	LVDS_TX0_N	22	TOUCH_XM
10	LVDS_TX0_P	23	TOUCH_YP
11	GND	24	TOUCH_YM
12	LVDS_TX1_N	25	+5V (fused)
13	LVDS_TX1_P		

7.7 J8, DVI Connector

Type: DVI-I connector

Pin	Signal	Pin	Signal	Pin	Signal
1	TMDS_D2_N	9	TMDS_D1_N	17	TMDS_D1_N
2	TMDS_D2_P	10	TMDS_D1_P	18	TMDS_D1_P
3	GND	11	GND	19	GND
4	n/c	12	n/c	20	n/c
5	n/c	13	n/c	21	n/c
6	n/c	14	+5V	22	GND
7	n/c	15	GND	23	TMDS_CLK_P
8	ANA_VSYNC	16	Hot Plug Detect	24	TMDS_CLK_N

C1	ANA_RED
C2	ANA_GREEN
C3	ANA_BLUE
C4	ANA_HSYNC
C5	GND

7.8 J10, Backlight Power Supply

Type: 2 pin header, 2.54 mm pitch

Pin	Signal
1	+5V
2	GND

7.9 J20 down, UART-A

Type: DSUB-9 male

Pin	Signal	Pin	Signal
1	n/c	6	n/c
2	UART_A_RXD#	7	UART_A_RTS#
3	UART_A_TXD#	8	UART_A_CTS#
4	n/c	9	n/c
5	GND		

7.10 J20 up, UART-B

Type: DSUB-9 male

Pin	Signal	Pin	Signal
1	n/c	6	n/c
2	UART_B_RXD#	7	n/c
3	UART_B_TXD#	8	n/c
4	n/c	9	n/c
5	GND		

7.11 J21, UART-C, D, E

Type: 2*6 pin header, 2.54 mm pitch

Pin	Signal	Pin	Signal
1	+3.3V	2	n/c
3	GND	4	n/c
5	UART_E_TXD	6	UART_C_RXD
7	UART_E_RXD	8	UART_C_TXD
9	UART_D_TXD	10	GND
11	UART_D_RXD	12	+3.3V

7.12 J5, Generic Camera Connector 1

Type: 2*13 pin header, 1.27 mm pitch

Pin	Signal	Pin	Signal
1	n/c	2	GND
3	+5 V	4	GND
5	CAM1_D0	6	CAM1_D1
7	CAM1_D2	8	CAM1_D3
9	CAM1_D4	10	CAM1_D5
11	CAM1_D6	12	CAM1_D7
13	GND	14	GND
15	CAM1_VD	16	PWRDOWN_CAM1#
17	CAM1_HD	18	GND
19	CAM1_CLK	20	RESET#
21	+3.3V	22	GND

23	SCL	24	SDA
25	+3.3V	26	GND

7.13 J6, Generic Camera Connector 2

Type: 2*13 pin header, 1.27 mm pitch

Pin	Signal	Pin	Signal
1	n/c	2	GND
3	+5 V	4	GND
5	CAM2_D0	6	CAM2_D1
7	CAM2_D2	8	CAM2_D3
9	CAM2_D4	10	CAM2_D5
11	CAM2_D6	12	CAM2_D7
13	GND	14	GND
15	CAM2_VD	16	PWRDOWN_CAM2#
17	CAM2_HD	18	GND
19	CAM2_CLK	20	RESET#
21	+3.3V	22	GND
23	SCL	24	SDA
25	+3.3V	26	GND

7.14 J16, Ethernet Connector

Type: Rj45 Jack (8 pin)

Pin	Signal
1	ETH_TDP
2	ETH_TDM
3	ETH_RDP
4	n/c
5	n/c
6	ETH_RDM
7	n/c
8	n/c

7.15 J3 (dual) & J4, USB Host Connector

Type: USB A connector (4 pin)

Pin	Signal
1	USBxH_VBUS
2	USBxH_DM
3	USBxH_DP
4	GND

x means 1, 2 and 3

7.16 J7, USB Device Connector

Type: USB B connector (4 pin)

Pin	Signal
1	USBF_VBUS
2	USBF_DM
3	USBF_DP
4	GND

7.17 J19, CAN connector

Type: 2*5 pin header, 2.54 mm pitch

Pin	Signal	Pin	Signal
1	+3.3V	2	n/c
3	GND	4	CAN2_RX
5	CAN1_TX	6	CAN2_TX
7	CAN1_RX	8	GND
9	n/c	10	+3.3V

7.18 J27, SATA connector

Type: Molex 67491-0020

Pin	Signal
1	GND
2	TXP
3	TXN
4	GND

5	RXN
6	RXP
7	GND

7.19 J25, I/O Extension Connector

Type: 2*11 pin header, 2.54 mm pitch

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	SCL	4	SDA
5	SPI_SS#	6	SPI_MISO
7	SPI_SCK	8	SPI_MOSI
9	CAN1_TX	10	CAN1_RX
11	GPIO_0	12	GPIO_1
13	GPIO_2	14	GPIO_3
15	GPIO_4	16	GPIO_5
17	GPIO_6	18	GPIO_7
19	GPIO_8	20	GPIO_9
21	GND	22	GND

7.20 J15, Analog Input

Type: 2*4-pin header, 2.54mm pitch

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	ANA_IN1	4	ANA_IN2
5	ANA_IN3	6	ANA_IN4
7	GND	8	GND

7.21 J11, Digital Audio, SPDIF

Type: 2*3-pin header, 2.54mm pitch

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	SPDIF OUT	4	SPDIF IN
5	GND	6	GND

7.22 J17, CPU Bus Connector

Type: 2*25 pin header, 1.27 mm pitch

Pin	Signal	Pin	Signal
1	+3.3V	2	GND
3	A14	4	A15
5	A12	6	A13
7	A10	8	A11
9	A8	10	A9
11	A6	12	A7
13	A4	14	A5
15	A2	16	A3
17	A0	18	A1
19	GND	20	GND
21	D14	22	D15
23	D12	24	D13
25	D10	26	D11
27	D8	28	D9
29	D6	30	D7
31	D4	32	D5
33	D2	34	D3
35	D0	36	D1
37	+3.3V	38	RESET#
39	CKIO	40	BS#
41	RD#	42	CS#
43	WE0#	44	WAIT#
45	WE1#	46	IRQ_B
47	I2C_SDA	48	I2C_SCL
49	+5V	50	GND

7.23 J31, Keypad

Type: 2*10-pin header, 2.54mm pitch

Pin	Signal	Pin	Signal
1	+3.3V	2	+3.3V
3	KEYPAD_ROW0	4	KEYPAD_COL0
5	KEYPAD_ROW1	6	KEYPAD_COL1
7	KEYPAD_ROW2	8	KEYPAD_COL2
9	KEYPAD_ROW3	10	KEYPAD_COL3
11	GND	12	GND
13	Reserved	14	GND
15	Reserved	16	GND
17	Reserved	18	GND
19	GND	20	GND

7.24 J23, RTC Battery Holder

Type: Battery Holder for CR1632

Pin	Signal
1	GND
2	BAT +

7.25 J24, DC Power Jack

Type: KLDX-SMT-0202AP

Pin	Signal
Center Tap	+5V
Outer Tap	GND

8 Technical Characteristics

8.1 Electrical Specifications

Electrical Specification	
Supply Voltage	+5V, +/-5%
Current consumption	max. 2.3A

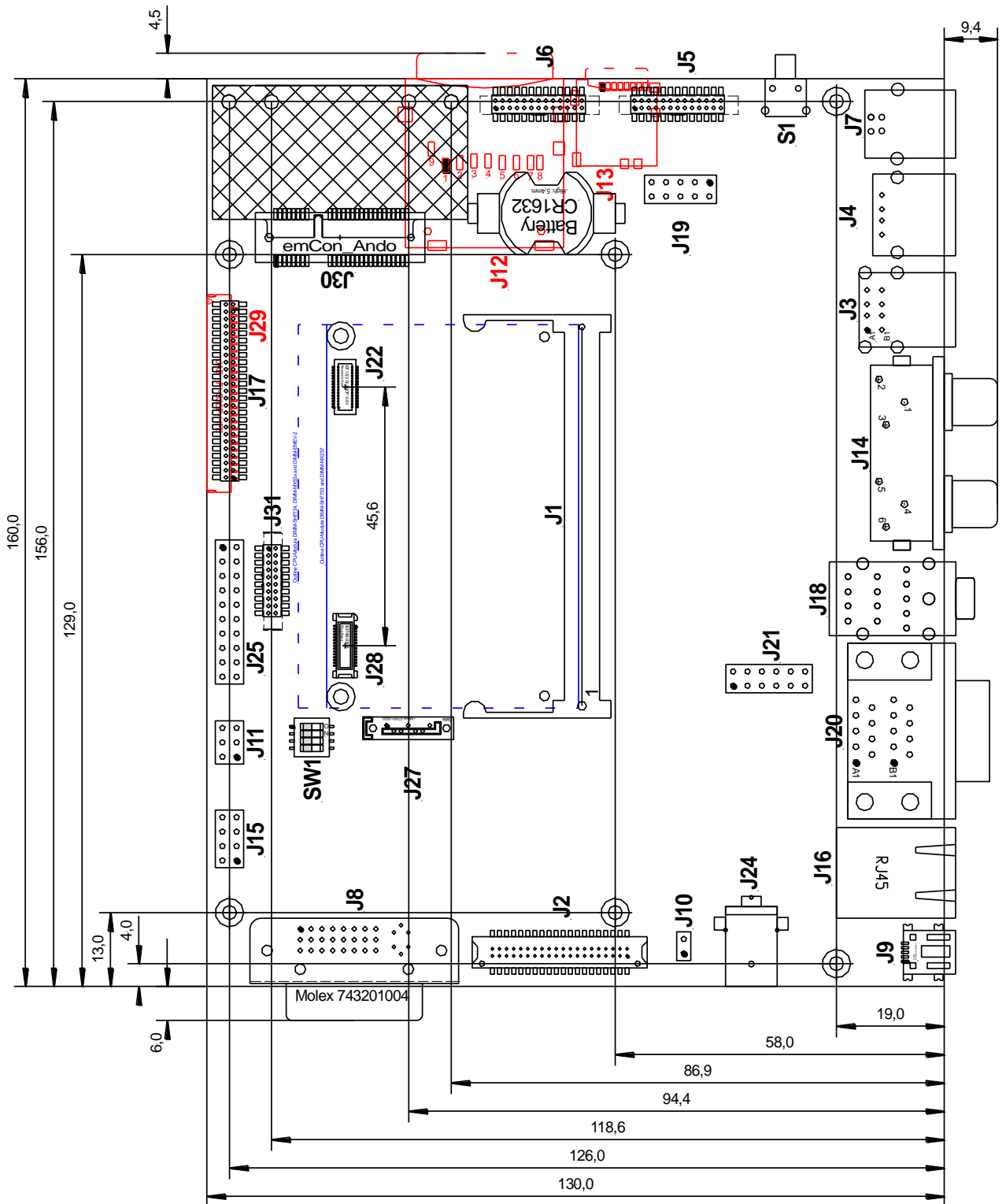
8.2 Environmental Specifications

Operating temperature	
Standard	0 ... +70°C
Extended	not available
Storage temperature	
Storage temperature	-40 ... +125°C
Relative humidity	
Relative humidity	0 ... 95 %, non-condensing

8.3 Mechanical Specifications

Mechanical Specifications	
Weight	approx. 200 g
Board	Glasepoxi FR-4, UL-listed, 8 layers
Dimensions	166 mm x 140 mm x 43 mm

9 Dimensional Drawing



Red colored parts are located on the bottom side of the CPU module.

The drill diameter of the six mounting holes is 2.5mm.

10 References

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- [8] TLV320AIC23B
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